REMARKS

Claims 1, 10, and 13 have been editorially amended, and claims 15-40 added. The attachment to this Amendment entitled "Version with Markings to Show Changes Made" is a marked-up version of the changes made to the claims. The Applicant has carefully and thoughtfully considered the Office Action and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

1. In the Office Action on pages 2-5 in section 2, claims 1-6 and 8-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,575,844 to Kosuge et al. (hereafter Kosuge). Applicant respectfully traverses this rejection.

The invention of the application, as defined by certain of the claims, teaches a switching mechanism where TDM and packet data can be switched by a single shared memory mechanism such that switching packet data has no latency or jitter effect on the TDM traffic. See, e.g., specification, page 5, 14-24. In an exemplary embodiment of the invention not necessarily recited in the claims, TDM and packet shared memory partitions and packet data queues per port contribute to the lack of latency or jitter effect on the TDM traffic. A varying amount of the single shared memory is used to store packet data, whereas the TDM portion of the shared memory is constant. Additionally, the use of routing information stored as part of a data exchange unit (DEU) assists in routing packet data. The switching of packet data by the shared memory has no latency or jitter effect on the switching of TDM data by the shared memory.

Amended claim 1 recites a switch for switching TDM data and packet data from input ports to output ports. The switch comprises a plurality of input ports, a plurality of output ports, and a single shared memory. The plurality of input ports receives data, and each data comprises

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either TDM data or packet data. The plurality of output ports transmits switched data. The single shared memory couples the input ports to the output ports and sequentially receives all TDM data and all the packet data from the input ports. The shared memory stores both TDM data and packet data. The shared memory switches all sequentially received TDM data and packet data from respective input ports to respective output ports. The switching of packet data by the shared memory has neither latency nor jitter effect on switching of TDM data by the shared memory, and the switching of TDM data is based on input time slots of said TDM data.

<u>Kosuge</u> teaches a digital switching system in Figure 1 having a hierarchical storage. The hierarchical storage includes a small-capacity high-speed memory 11, a large-capacity low-speed memory 12, and a file memory 13. For circuit switching, the memory 11 is used. <u>Kosuge</u>, column 1, lines 64-66; column 3, lines 29-35; column 6, lines 4-8 and 15-18; Figures 4 and 5. For packet switching, the memory 11, the memory 12, and the memory 13 are used. <u>Kosuge</u>, column 1, lines 64-66; column 3, lines 29-39; column 6, lines 8-14 and 18-25; Figures 4 and 5. <u>Kosuge</u>, however, fails to teach at least <u>**five**</u> aspects of amended claim 1.

First, <u>Kosuge</u> fails to teach a <u>**single**</u> shared memory. Claim 1 is amended to recite only <u>**one**</u> memory, specifically a <u>**single**</u> shared memory. In rejecting claim 1, the Office Action aligns the recited shared memory with the hierarchical storage 10 in Figure 1 of <u>Kosugue</u>. The hierarchical storage 10 of <u>Kosugue</u>, however, consists of <u>**three separate and distinct memories**</u>, namely the small-capacity high-speed memory 11, the large-capacity low-speed memory 12, and the file memory 13. <u>Kosuge</u>, Figure 1; column 3, lines 24-27; column 6, lines 8-25. For circuit switching, the small-capacity high-speed memory 11 is used. <u>Kosuge</u>, column 1, lines 64-66; column 3, lines 29-35; column 6, lines 4-8 and 15-18; Figures 4 and 5. For packet switching, the small-capacity high-speed memory 11, the large-capacity low-speed memory 12, and the file

memory 13 are used. Kosuge, column 1, lines 64-66; column 3, lines 29-39; column 6, lines 8-14 and 18-25; Figures 4 and 5. The hierarchical storage 10 of Kosuge is **not** a **single** memory and is, instead **three** memories. Hence, Kosuge fails to teach a single memory.

Second, Kosuge fails to teach a **single** shared memory to switch **all** TDM data and **all** packet data. Claim 1 is amended to recite specifically a **single** shared memory to switch **all** of the data. In rejecting claim 1, the Office Action aligns the recited shared memory with the hierarchical storage 10 in Figure 1 of Kosugue. As noted above, the hierarchical storage 10 of Kosugue consists of **three separate and distinct memories**, namely the small-capacity high-speed memory 11, the large-capacity low-speed memory 12, and the file memory 13. Kosuge, Figure 1; column 3, lines 24-27; column 6, lines 8-25. Although the small-capacity high-speed memory 11 performs both circuit switching and packet switching of data, **all** of the packet switching is **not** performed by the small-capacity high-speed memory 11 of Kosuge. Instead, the packet switching of Kosuge requires **two additional memories**, namely the large-capacity low-speed memory 12 and the file memory 13. The three memories 11, 12, and 13 of Kosuge have different speeds (i.e., high speed for memory 11, and low speed for memory 12) and different sizes (i.e., small capacity for memory 11, and large capacity for memory 13). Kosuge, Figure 1; column 3, lines 24-27. The system of Kosuge requires **three** different and unique memories to implement the switching of **all** circuit data and **all** packet data, whereas the claimed invention requires only a **single** shared memory to switch **all** TDM data and **all** packet data. Hence, Kosuge fails to teach the recited single shared memory switching all TDM data and all packet data.

Third, Kosuge fails to teach a **single** shared memory storing **both** TDM data and packet data and switching **all** TDM data and **all** packet data. Claim 1 is amended to recite specifically a

single shared memory storing **both** TDM data and packet data and switching **all** of the data. In rejecting claim 1, the Office Action aligns the recited shared memory with the hierarchical storage 10 in Figure 1 of Kosugue. Although the small-capacity high-speed memory 11 performs stores both circuit data and packet data, the small-capacity high-speed memory 11 does **not** switch **all** circuit data and **all** packet data. Kosuge, column 3, lines 29-35; column 6, lines 4-8 and 15-18; Figures 4 and 5. Instead the task of switching all packet data is shared with the large-capacity low-speed memory 12 and the file memory 13. However, the large-capacity low-speed memory 12 stores **only** packet data and does **not** store circuit data, and the file memory 13 likewise stores **only** packet data and does **not** store circuit data. Kosuge, column 3, lines 35-39; column 6, lines 8-14 and 18-25; Figures 4 and 5. Hence, Kosuge fails to teach a single shared memory storing both TDM data and packet data and switching all TDM data and all packet data.

Fourth, Kosuge fails to teach switching of TDM data based on **input time slots** of the TDM data as recited in amended claim 1. Instead, Kosuge teaches in Figure 1 switching of circuit data based on **control data extracted** from a **common control channel signal** received by a signal reception circuit 17 from the TDM transmission input lines 15. Kosuge, column 3, line 66, to column 4, line 4. Under control of the processor 18 in Figure 1 of Kosuge, the control section 14 switches TDM data based on the control data extracted from the common control channel signal. Kosuge, column 4, lines 4-6. As illustrated in Figure 2 of Kosuge, the control data extracted from the common control channel signal includes **five data types**: a service indicator A indicating circuit switching or packet switching; a terminal indicator B indicating the terminal type for circuit switching or packet switching; a signal indicator C including supervisory signals, such as an originating signal, a disconnect signal, and an off-hook signal; a rate indicator D including transmission rate data; and a selection data E including a dialing

signal. Kosuge, column 4, lines 7-23. **None** of these five data types of Kosuge correspond the recited input time slots of TDM data. Kosuge teaches switching of circuit data based on these five data types of the control data extracted from the common control channel signal and **not** based on input time slots of the TDM data. Hence, Kosuge fails to teach switching of TDM data based on input time slots of the TDM data.

Fifth, Kosuge fails to teach the avoidance of latency and jitter effects on the switching of TDM data by a shared memory due to the switching of packet data by the shared memory. In rejecting claim 1, the Office Action relies on the teachings of Kosugue at column 1, lines 64-67, and Figure 5. **Neither** of these citations address latency and jitter effects of switching. Kosugue teaches at column 1, lines 64-67, using three separate and distinct memories for circuit and packet switching. In Figure 5, Kosuge illustrates using the three separate and distinct memories to switch circuit data and packet data. Kosugue, column 6, lines 1-32. **Nowhere** in these citations does Kosuge mention, or even fairly suggest, the latency and jitter effects of switching.

Instead, at column 3, lines 13-16, Kosuge recognizes that packet data switching imparts non-constant delays in a switching system. Although Kosuge recognizes non-constant delays for switching packet data, Kosuge fails to recognize that **jitter effects** can **also** occur in such a system. Kosuge, column 3, lines 13-16. Additionally, the system of Kosuge is **not** described as minimizing latency effects and jitter effects on the switching of circuit data. Moreover, Kosuge fails to teach the avoidance of **both** latency **and** jitter effects as addressed by the present invention. Indeed, Kosuge seemingly fails to appreciate the need to avoid the impact of packet processing on TDM latency and jitter. Therefore, amended claim 1 is allowable over Kosuge.

Claims 2-9 and 14 are dependent from amended claim 1 and are allowable as being dependent from an allowable claim.

Further, claim 5 recites that the shared memory places sequentially received packet data in a queue for a respective output port. The use of queues for packet data and the ordered withdrawal of packet data from a queue are discussed in the application, for example, on page 11 at lines 10-13 and 20-23. In contrast, Kosuge teaches using **buffers** to store packet data. Kosuge, Figure 5, buffers in 12 and 13; column 6, lines 8-14 and 18-25. Kosuge fails to teach the ordered withdrawal data from the buffers, as required for withdrawing data from a queue. Kosuge provides no explanation as to how data is input and output from the buffers. For example, Kosuge does not disclose whether or not the buffer includes header pointers and link lists, as can be used in a queue. Hence, Kosuge fails to teach a queue for packet data.

Claim 6 recites that the data received by the input and transmitted by the output ports are data exchange units. See, e.g., specification, page 5, line 5, to page 6, line 9. For packet data, the data exchange units can include header information. See, e.g., specification, page 12, lines 18-29. In contrast, Kosuge fails to mention or even refer to the concept of "exchange units" or "data exchange units." Instead, Kosuge teaches the usage of **time slots** on the input and output time division transmission lines 15 and 16. Kosuge, column 3, lines 31-32; column 5, line 63, to column 6, line 4; Figures 4 and 5. Additionally, Kosuge fails to teach using control information **within the timeslot data itself** to control the writing of the data into and reading of the data out of the three memories 11, 12, and 13, as well as between the input ports and the output ports. The recited data exchange units are **not** the same as the timeslots of Kosuge. Hence, Kosuge fails to teach data exchange units.

Amended claim 10 recites subject matter similar to the allowable subject matter recited in amended claim 1 and is allowable over Kosuge for reasons similar to those discussed above for amended claim 1 for the similar limitations.

Further, claim 10 is amended to recite limitations similar to some of the allowable limitations recited in allowable claim 7. Hence, claim 10 is allowable as reciting similar allowable subject matter.

Claims 11 and 12 are dependent from claim 10 and are allowable as being dependent from an allowable claim.

Further, claim 12 recites that the output port to which TDM data is routed is determined based on a time slot in a frame in which the TDM data was received by the input port, and that the output port to which the packet data is routed is determined based on routing data embedded in the packet data and based on the input port which received the packet data. The use of routing data embedded in the packet data is discussed in the specification, for example, on page 12 at lines 18-22. In contrast, Kosuge teaches using a **separate** time division multiplex control channel to direct the switching based on the time slot that the data arrives on the input port. Kosuge, column 6, lines 61 ff; Figure 3, blocks 100, 101, and 102; Figure 6, blocks 17R, 401, 402, 408, 404, and 403. Using the control channel to direct switching as in Kosuge is **not** the same as using routing date embedded in the packet data, as recited in claim 12. Hence, Kosuge fails to teach the routing of packet data as recited.

Claim 13 recites subject matter similar to the allowable subject matter recited in amended claim 1 and is allowable over Kosuge for reasons similar to those discussed above for amended claim 1 for the similar limiations.

Further, claim 13 is amended to recite limitations similar to some of the allowable limitations recited in allowable claim 7. Hence, claim 13 is allowable as reciting similar allowable subject matter.

In addition to being dependent from an allowable claim, namely claim 1, claim 14 recites that data is received by the input ports and transmitted by the output ports as data exchange units. The data exchange units are packet data comprising routing information. Switching of a data exchange unit from a respective input port to a respective output port is controlled by a stored switch configuration. The stored switch configuration uses the routing information of data exchange units for packet data to determine respective output ports to switch the data exchange units. As discussed above for claims 6 and 12, <u>Kosuge</u> fails to teach using data exchange units and using routing data embedded in the packet data. For the same reasons discussed above for claims 6 and 12, <u>Kosuge</u> fails to teach the limitations recited in claim 14.

2. In the Office Action on page 5 in section 4, claim 7 is objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form. The Applicant thanks the Examiner for the indication of allowable subject matter. Claim 7 has been rewritten in independent form as added claim 15, and claim 15 is, hence, allowable. Claims 16-20 depend from claim 15 and are allowable as being dependent from an allowable claim.

3. Claims 21-40 are additionally added. Claims 21, 31, 34, and 35 are independent claims. Claims 22-30 depend from claim 21, claims 32-33 depend from claim 31, and claims 36-40 depend from claim 35.

4. The fee of $696 is being submitted herewith for four additional independent claims in excess of three (4 x $84 = $336) and twenty additional claims in excess of twenty (20 X $18 =

$360). If no check is attached, or if a greater or lesser fee is required, please charge or credit Deposit Account Number 22-0261 accordingly and notify the undersigned.

THEREFORE, because all rejections have been overcome, it is submitted that claims 1-40 are allowable, and such allowance is requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1, 10, and 13 are amended as follows:

1. (Amended) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

a plurality of input ports receiving data, wherein each data comprises either TDM data or packet data;

a plurality of output ports transmitting switched data; and

a single shared memory coupling said input ports to said output ports, said single shared memory sequentially receiving all TDM data and all packet [the] data from said input ports, said single shared memory storing both TDM data and packet data, said single shared memory switching [a] all sequentially received TDM data and packet data from [a] respective input ports to [a] respective output ports, wherein switching of packet data by said single shared memory has neither [no] latency nor jitter effect on switching of TDM data by said single shared memory, and wherein switching of TDM data is based on input time slots of said TDM data.

10. (Amended) A method for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising the steps of:

switching a TDM data from an input port to an output port, comprising the steps of:

receiving a TDM data at the input port;

determining the output port to route the TDM data;

selecting an address of a single shared memory for the TDM data based on a time slot of a frame in which the TDM data was received;

storing the TDM data at the address in said [in a preselected area of a] shared memory;

reading the TDM data from the address in [preselected area of] said shared memory; and

transmitting the TDM data from the output port; and

switching a packet data from an input port to an output port, comprising the steps of:

receiving a packet data at the input port;

determining the output port to route the packet data;

selecting an address of said single shared memory for the packet data based on routing data embedded in the packet data and based on the input port which received the packet data;

storing the packet data at the address in said shared memory;

reading the packet data from the address in said shared memory; and

transmitting the packet data from the output port;

wherein switching packet data has neither [no] latency nor jitter effect on switching TDM data.

13. (Amended) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

means for switching a TDM data from an input port to an output port, comprising:

means for receiving a TDM data at the input port;

means for determining the output port to route the TDM data;

<u>means for selecting an address of a single shared memory for the TDM data based on a time slot of a frame in which the TDM data was received;</u>

means for storing the TDM data <u>at the address in said</u> [in a preselected area of a] shared memory;

means for reading the TDM data from the <u>address in</u> [preselected area of] said shared memory; and

means for transmitting the TDM data from the output port; and

means for switching a packet data from an input port to an output port, comprising:

means for receiving a packet data at the input port;

means for determining the output port to route the packet data;

<u>means for selecting an address of said single shared memory for the packet data based on routing data embedded in the packet data and based on the input port which received the packet data;</u>

means for storing the packet data <u>at the address</u> in said shared memory;

means for reading the packet data from <u>the address in</u> said shared memory; and

means for transmitting the packet data from the output port;

wherein switching packet data has <u>neither</u> [no] latency <u>n</u>or jitter effect on switching TDM data.

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